L Number	Hits	Search Text	DB	Time stamp
29	187860	((transistor with (drain source channel)) with implantation implant$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:07
30	11490	(((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:08
31	812	((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:09
32	288	(((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities)) and stress$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:11
33	157	((((((transistor with (drain source channel)) with implantation implant$3)) and (implant$5 with (void cavity cavities buble $5buble gas$2))) and (mobility mobilities)) and stress$3) and (compress$3 tensile)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:11
34	11088	(((transistor with (drain source channel)) with implantation implant$3)) and ((implant$2 implantation implanting) with (void cavity cavities buble $5buble gas$2))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:07
35	19353	transistor with (implantation implant$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:08
37	989	(transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:09
38	416	((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:10
39	399	(((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:10
40	356	((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source) and drain	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:10
41	351	(((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source) and drain) and region	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:10

42	316	((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source) and drain) and region) and channel	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:11
43	130	(((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source) and drain) and region) and channel) and stress$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:11
44	45	((((((((transistor with (implantation implant$3)) and (void cavity cavities buble $5buble)) and (mobility mobilities carrier)) and source) and drain) and region) and channel) and stress$3) and (compress$3 tensile)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:23
45	1		USPAT	2003/05/12 14:16
46	1		USPAT	2003/05/12 14:16
47	610	(transistor with (implantation implant$3)) and void	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:24
50	0	((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (buble $5buble))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:26
49	5	((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (cavit$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:26
48	91	((transistor with (implantation implant$3)) and void) and ((implanting implantation implant$2) with (void))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/05/12 14:27
51	1		USPAT	2003/05/12 14:52
52	1		USPAT	2003/05/12 14:53
53	1		USPAT	2003/05/12 14:53

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L49: (5) 47 and ((implanting implantation implant$2) with (cavit$3))
L48: (91) 47 and ((implanting implantation implant$2) with (void))
L51: (1) "5953622".PN.

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1			US 20020135041 A1	20020926	41	Semiconductor integrated circuit and semiconductor device	257/510	257/E27.085; 257/E29.134;
2			US 20020127841 A1	20020912	21	Method of manufacturing semiconductor device	438/620	
3			US 20020096496 A1	20020725	15	Patterning of GaN crystal films with ion beams and subsequent wet etchin	216/87	
4			US 20020074598 A1	20020620	12	Methodology for control of short channel effects in MOS transistors	257/345	257/349
5			US 20020034865 A1	20020321	36	Semiconductor device and method of fabricating the same	438/514	438/527; 438/528;
6			US 20020001960 A1	20020103	89	Material removal method for forming a structure	438/705	257/E27.089; 438/704
7			US 20010015466 A1	20010823	22	Semiconductor device and method for producing same	257/401	
8			US 20010008787 A1	20010719	16	Method of forming complementary type conductive regions on a substrat	438/258	438/264
9			US 20010008297 A1	20010719	22	Semiconductor device and method for producing same	257/506	
10			US 20010001500 A1	20010524	22	Semiconductor device and method for producing same	257/506	
11			US 6503799 B2	20030107	19	Method of manufacturing semiconductor device	438/269	438/341; 438/412;
12			US 6465290 B1	20021015	27	Method of manufacturing a semiconductor device using a polyme	438/183	257/407

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
13	☐	☐	US 6461967 B2	20021008	86	Material removal method for forming a structure	438/705	216/38; 216/87;
14	☐	☐	US 6362082 B1	20020326	13	Methodology for control of short channel effects in MOS transistors	438/523	257/E21.335; 257/E21.339;
15	☐	☐	US 6350638 B1	20020226	16	Method of forming complementary type conductive regions on a substrat	438/199	257/E21.637; 257/E21.638;
16	☐	☐	US 6333217 B1	20011225	36	Method of forming MOSFET with channel, extension and pocket implan	438/197	257/E21.435; 257/E21.437;
17	☐	☐	US 6309975 B1	20011030	91	Methods of making implanted structures	438/705	216/38; 216/87;
18	☐	☐	US 6291311 B1	20010918	20	Semiconductor device and method for producing same	438/439	257/E21.552; 257/E21.555;
19	☐	☐	US 6281532 B1	20010828	13	Technique to obtain increased channel mobilities in NMOS transisto	257/288	257/418; 257/E21.195;
20	☐	☐	US 6281081 B1	20010828	7	Method of preventing current leakage around a shallow trench isolation stru	438/296	257/E21.546; 438/424;
21	☐	☐	US 6261964 B1	20010717	91	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
22	☐	☐	US 6259118 B1	20010710	14	Ultra high density NOR gate using a stacked transistor arrangement	257/67	257/365; 257/369
23	☐	☐	US 6255181 B1	20010703	12	Method for fabricating MOS semiconductor device having salicide	438/305	
24	☐	☐	US 6228694 B1	20010508	14	Method of increasing the mobility of MOS transistors by use of localized s	438/199	257/E21.618; 257/E21.619;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
25			US 6214700 B1	20010410	19	Semiconductor device and method for producing same	438/450	257/374; 257/E21.552;
26			US 6201278 B1	20010313	28	Trench transistor with insulative spacers	257/330	257/332; 257/336;
27			US 6200842 B1	20010313	17	Method of forming complementary type conductive regions on a substrat	438/199	257/E21.637; 257/E21.638;
28			US 6191019 B1	20010220	14	Method for forming a polysilicon layer in a polycide process flow	438/592	257/E21.2; 438/586;
29			US 6188110 B1	20010213	11	Integration of isolation with epitaxial growth regions for enhanced device f	257/368	257/336; 257/337;
30			US 6100146 A	20000808	28	Method of forming trench transistor with insulative spacers	438/301	257/E21.429; 257/E29.13;
31			US 6075268 A	20000613	12	Ultra high density inverter using a stacked transistor arrangement	257/327	257/365; 257/369;
32			US 6074902 A	20000613	16	Method of forming complementary type conductive regions on a substrat	438/199	257/E21.637; 257/E21.638;
33			US 6072222 A	20000606	11	Silicon implantation into selective areas of a refractory metal to reduce	257/383	257/757; 257/E21.165;
34			US 6057194 A	20000502	28	Method of forming trench transistor in combination with trench array	438/270	257/E21.428; 257/E21.429;
35			US 6054370 A	20000425	11	Method of delaminating a pre-fabricated transistor layer from a	438/456	257/E21.568; 438/457;
36			US 6037629 A	20000314	13	Trench transistor and isolation trench	257/333	257/330; 257/397;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
37			US 6025633 A	20000215	8	Multi-level transistor fabrication method having an inverted, upper leve	257/369	257/343; 257/350;
38			US 6005272 A	19991221	21	Trench transistor with source contact in trench	257/344	257/330; 257/332;
39			US 5986311 A	19991116	21	Semiconductor device having recrystallized source/drain regions	257/382	257/347; 257/66;
40			US 5970331 A	19991019	13	Method of making a plug transistor	438/199	257/274; 257/369;
41			US 5962894 A	19991005	21	Trench transistor with metal spacers	257/330	257/332; 257/336;
42			US 5960268 A	19990928	22	Semiconductor device and method of fabricating the same	438/166	257/E21.415; 257/E29.277;
43			US 5929495 A	19990727	25	Semiconductor processing method of forming a static random access mem	257/392	257/402; 257/647;
44			US 5923980 A	19990713	16	Trench transistor with localized source/drain regions implanted throug	438/270	257/262; 257/E21.205;
45			US 5905285 A	19990518	11	Ultra short trench transistors and process for making same	257/344	257/395; 257/396;
46			US 5888880 A	19990330	19	Trench transistor with localized source/drain regions implanted throug	438/424	257/E21.429; 257/E29.267;
47			US 5882959 A	19990316	9	Multi-level transistor fabrication method having an inverted, upper leve	438/152	257/E21.614; 257/E27.026;
48			US 5874341 A	19990223	22	Method of forming trench transistor with source contact in trench	438/301	257/E21.205; 257/E21.427;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
49	□	□	US 5872059 A	19990216	16	Method of forming complementary type conductive regions on a substrat	438/692	216/38; 257/E21.637;
50	□	□	US 5872029 A	19990216	11	Method for forming an ultra high density inverter using a stacked transi	438/152	257/E21.614; 257/E27.026;
51	□	□	US 5863818 A	19990126	11	Multilevel transistor fabrication method having an inverted, upper leve	438/152	257/E21.614; 257/E27.026;
52	□	□	US 5834354 A	19981110	13	Ultra high density NOR gate using a stacked transistor arrangement	438/305	438/306
53	□	□	US 5824576 A	19981020	15	Method of forming complementary type conductive regions on a substrat	438/199	257/E21.637; 257/E21.638;
54	□	□	US 5817560 A	19981006	11	Ultra short trench transistors and process for making same	438/301	257/E21.429; 257/E29.267
55	□	□	US 5807771 A	19980915	8	Radiation-hard, low power, sub-micron CMOS on a SOI substrat	438/154	257/E21.703; 257/E27.112;
56	□	□	US 5801075 A	19980901	23	Method of forming trench transistor with metal spacers	438/197	257/E21.429; 257/E29.122;
57	□	□	US 5796143 A	19980818	28	Trench transistor in combination with trench array	257/330	257/374; 257/E21.429;
58	□	□	US 5780340 A	19980714	12	Method of forming trench transistor and isolation trench	438/259	257/E21.428; 257/E21.429;
59	□	□	US 5763319 A	19980609	10	Process for fabricating semiconductor devices with shallowly	438/514	257/E21.143; 257/E21.335;
60	□	□	US 5753548 A	19980519	8	Method for preventing fluorine outgassing-induced interlevel dielectri	438/231	438/552

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
61			US 5751046 A	19980512	24	Semiconductor device with V.sub.T implant	257/392	257/402; 257/647;
62			US 5714394 A	19980203	13	Method of making an ultra high density NAND gate using a stacked tr	438/199	257/E21.614; 257/E27.026;
63			US 5707896 A	19980113	7	Method for preventing delamination of interlevel dielectric layer over FET	438/231	438/660
64			US 5654218 A	19970805	10	Method of manufacturing inverse t-shaped transistor	438/301	257/E21.434; 257/E29.135;
65			US 5600586 A	19970204	19	Flat-cell ROM and decoder	365/104	365/63
66			US 5567966 A	19961022	5	Local thinning of channel region for ultra-thin film SOI MOSFET with ele	257/347	257/350; 257/382;
67			US 5427963 A	19950627	9	Method of making a MOS device with drain side channel implant	438/257	257/E21.427; 257/E21.682;
68			US 5350702 A	19940927	6	Method for fabricating a dual-gate metal-semiconductor field effect trans	438/176	148/DIG.73; 257/E21.455;
69			US 5270227 A	19931214	17	Method for fabrication of semiconductor device utilizing ion im	438/234	148/DIG.1; 148/DIG.10;
70			US 5223445 A	19930629	15	Large angle ion implantation method	438/302	257/E21.335; 257/E21.336;
71			US 5182225 A	19930126	66	Process for fabricating BICMOS with hypershallow junctions	438/202	257/276; 257/370;
72			US 5171713 A	19921215	66	Process for forming planarized, air-bridge interconnects on a semicon	438/31	148/DIG.20; 257/750;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
73			US 5134083 A	19920728	66	Method of forming self-aligned contacts in a semiconductor process	438/234	148/DIG.19; 438/233
74			US 5132237 A	19920721	66	Planarization method for fabricating high density semiconductor devices	438/294	438/1; 438/359
75			US 5112761 A	19920512	68	BiCMOS process utilizing planarization technique	438/207	257/370; 257/E21.193;
76			US 5108945 A	19920428	66	Process for fabricating polysilicon resistors and interconnects	438/384	148/DIG.136; 257/E21.193;
77			US 5023190 A	19910611	11	CMOS processes	438/200	257/369; 257/408;
78			US 4874714 A	19891017	9	Method of making laterally oriented Schottky diode	438/200	257/384; 257/476;
79			US 4784965 A	19881115	18	Source drain doping technique	438/303	148/DIG.106; 148/DIG.53;
80			US 4757026 A	19880712	18	Source drain doping technique	438/231	148/DIG.106; 148/DIG.82;
81			US 4728617 A	19880301	16	Method of fabricating a MOSFET with graded source and drain regions	438/305	148/DIG.106; 148/DIG.53;
82			US 4719185 A	19880112	12	Method of making shallow junction complementary vertical bipolar transis	438/322	257/525; 257/574;
83			US 4398964 A	19830816	6	Method of forming ion implants self-aligned with a cut	438/526	257/E21.024; 257/E21.346;
84			US 3841918 A	19741015	11	METHOD OF INTEGRATED CIRCUIT FABRICATION	438/331	148/DIG.117; 148/DIG.85;

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
81	☐	☐	US 4728617 A	19880301	16	Method of fabricating a MOSFET with graded source and drain regions	438/305	148/DIG.106; 148/DIG.53;
82	☐	☐	US 4719185 A	19880112	12	Method of making shallow junction complementary vertical bipolar transis	438/322	257/525; 257/574;
83	☐	☐	US 4398964 A	19830816	6	Method of forming ion implants self-aligned with a cut	438/526	257/E21.024; 257/E21.346;
84	☐	☐	US 3841918 A	19741015	11	METHOD OF INTEGRATED CIRCUIT FABRICATION	438/331	148/DIG.117; 148/DIG.85;
85	☐	☐	US 6448163 B	20020910	10	Fabrication of T-shaped gate for transistor involves defining base lengt		
86	☐	☐	US 6362082 B	20020326	13	Improvement of short channel effect in transistor involves implanting subst		
87	☑	☐	US 6228694 B	20010508		Carrier mobility modifying method for transistor involves forming channe		
88	☑	☐	US 6191019 B	20010220		Prevention of void formation in gate of transistor formed in substrate com		
89	☑	☐	US 6188110 B	20010213		Integrated circuit, e.g. metal oxide semiconductor devices, includes isola		
90	☑	☐	US 5807771 A	19980915		Radiation hard, low power, sub-micron CMOS devices - fabricat		
91	☑	☐	US 5753548 A	19980519		Forming N-channel and P-channel FETs, especially for CMOS circuits -		

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